Amendments to the Specification:

Please replace the paragraphs starting on page 5 of the amended specification, line 29, to page 6, line 24 with the following amended paragraph:

-- The discriminator unit DE is connected via an output AP to an input EL of a loop filter LF, which is, in turn, connected via an output AL to an input EV of a voltage controlled oscillator VCO. A first and a second variable digital frequency divider T1,T2 is each connected via an input (ET1, ET2) to an output AV of the voltage controlled oscillator VCO. The first digital frequency divider T1 is connected to a clock input CLK of the phase discriminator PD, and the second digital frequency divider T2 is connected to a divider input ETF of the frequency window discriminator FD, in each case via an output ~~AT~~AT2. The described discriminator unit DE, including a phase window discriminator PD and a frequency window discriminator FD, as well as the loop filter LF, the voltage controlled oscillator VCO and the two variable digital frequency dividers T1, T2 are functional components of a generally known phase locked loop, whose function for recovery of the clock from the data stream ds passed to it in addition to the sampling of the data stream ds to be regenerated in conjunction with the sampling flipflop AFF are sufficiently well known to those skilled in the art, and will not be described in any more detail in the following text.

The phase/frequency control device PLL has a clock output CA which is connected to the output ~~AT~~ AT1 of the first frequency divider T1, and to which the clock signal ts which is produced is passed. The output ~~AT~~ AT1 of the first frequency divider T1 is, in turn, connected to a clock input CLK of the sampling flipflop AFF. The sampling flipflop AFF is connected via an output AF to a data output ~~AT~~ ATP of the phase/frequency control device PLL, to which the data stream cds, regenerated via the sampling flipflop AFF, is passed. Furthermore, the output AF of the sampling flipflop AFF is connected to an input ~~ES~~ ESR of a shift register SR arranged in the frame identification unit RD. The shift register SR has a clock input CLK which is connected to the output ~~AT~~ AT1 of the first frequency divider T1. –

Please replace the paragraphs starting on page 7of the amended specification, lines 12-22 with the following amended paragraph:

-- The control unit STRG is connected via a data bus DB having a number of data lines to a memory register MR, which is arranged in the frame identification unit RD and to which protocol identification information PID1...n which is stored in the memory MEM can be transmitted and stored therein, indicated by a rectangle with a dashed outline. The shift register SR and the memory register MR are connected via respective outputs AS, AM and a respective number of data lines DL1...n to corresponding inputs EC of a comparator unit COMP. The comparator COMP has comparison capabilities which are used to compare the binary information or data words applied to the inputs EC, and the comparison result is transmitted in the form of a data signal int via an output AC and a signaling line SCS to an input ~~ES~~ ESG of the control unit STRG. --

Please replace the paragraph starting on page 9, line 23 to page 10, line 8, with the following amended paragraph:

-- As already explained, the phase locked loop which is arranged in the phase/frequency control device PLL is matched to the data transmission rate of the incoming digital data stream ds via the control loop control information PLL_WORD1 stored in the register unit REG. By way of example, the transmission of appropriate control information si2,3 via the control lines SL2 and SL3 sets the controllable frequency dividers T1, T2 such that the frequency of the signal delivered from the voltage controlled oscillator VCO is divided as appropriate for matching of the optimum operating point of the phase discriminator PD and of the frequency window discriminator FD. Additional control information, in this case si4, transmitted via the fourth control line SL4 is used to provide any possibly required presetting or switching of the voltage controlled oscillator VCO. According to one alternative embodiment of the circuit arrangement, a number of voltage controlled oscillators VCO can be arranged in the phase/frequency control device PLL, in which case one voltage controlled oscillator VCO, which is matched to the data

transmission rate of the incoming digital data stream ds, in each ~~can case~~case can be selected with the aid of the fourth control signal si4. --

Please delete the Abstract of the Disclosure on page 13, lines 14-23, and enter the following Abstract of the Disclosure on a separate page:

-- ABSTRACT OF THE DISCLOSURE

A method and system for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop, wherein in a synchronization process by means of the phase locked loop, a data signal is sampled successively using a clock signal at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information associated with the selected clock signal, until protocol identification information is detected such that the frequency resolution of the phase locked loop is advantageously increased, and the synchronization of the clock signal to the data signal is improved. --